TRANSMITTAL OF APPEAL BRIEF

Docket No. SON-1582/SUG

In re Application of: Masumitsu Ino et al.

Application No.	Filing Date	Examiner	Group Art Unit
09/424,544-Conf. #8128	November 24, 1999	J. J. Piziali	2673

Invention: LIQUID CRYSTAL DISPLAY

TO THE COMMISSIONER OF PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed: February 4, 2004 .

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Dated: April 2, 2004

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Masumitsu Ino et al.

Application No.: 09/424,544 Confirmation No.: 8128

Filed: November 24, 1999 Art Unit: 2673

For: LIQUID CRYSTAL DISPLAY Examiner: J. J. Piziali

APPELLANT'S BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is an Appeal Brief under Rule 192 appealing the final decision of the Examiner dated November 4, 2003. Each of the topics required by Rule 192 is presented herewith and is labeled appropriately.

This brief is in furtherance of the Notice of Appeal, filed in this case on February 4, 2004.

This brief is transmitted in triplicate.

This brief contains items under the following headings as required by 37 C.F.R. § 1.192 and M.P.E.P. § 1206:

I. Real Party In Interest
II Related Appeals and Interferences
III. Status of Claims
IV. Status of Amendments
V. Summary of Invention

VI. Issues
VII. Grouping of Claims
VIII. Arguments
IX. Claims Involved in the Appeal
Appendix A Claims

I. REAL PARTY IN INTEREST

Sony Corporation of Tokyo, Japan ("Sony") is the real party in interest of the present application. An assignment of all rights in the present application to Sony was executed by the inventor and recorded by the U.S. Patent and Trademark Office at **reel 010555, frame 0866.**

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

Claims 1-20 were originally filed in this application.

III. STATUS OF CLAIMS

By the amendment filed on February 27, 2002, claims 9 and 16 have been amended, and claims 21-39 added.

By the amendment filed on September 16, 2002, claims 3 and 38 have been amended, and claims 40-42 added.

By the amendment filed on February 26, 2003, claims 1-2, 10, 12-13, 21-22, 30, 32-36, and 38-42 have been canceled, claims 3, 11, 13, 15, 17-20, 25-27 and 37 have been amended, and claims 43-48 added.

By the amendment filed on August 20, 2003, claim 3 has been amended.

The Amendment After Final Rejection Under 37 C.F.R. § 1.116 filed on February 4, 2004 proposed the cancellation of claims 3, 5, 7, 11, 13-20 and 23-42, proposed an amendment to claims 6 and 25, and proposed the addition of claims 49-66. However, the Advisory Action of February 25, 2004 indicated that the Amendment After Final Rejection Under 37 C.F.R. § 1.116 of February 4, 2004 had not been entered.

The Second Amendment After Final Rejection Under 37 C.F.R. § 1.116 filed on March 8, 2004 proposed the cancellation of claims 3, 5, 7, 11, 13-20 and 23-42, proposed an amendment to claims 6 and 25, and proposed the addition of claims 49-60. The Third Amendment After Final Rejection Under 37 C.F.R. § 1.116 filed on March 8, 2004 proposed the addition of claims 61-66.

However, the Advisory Action of February 25, 2004 indicated that the Amendment After Final Rejection Under 37 C.F.R. § 1.116 of February 4, 2004 had not been entered. No Advisory Action regarding the Second and Third Amendments After Final Rejection Under 37 C.F.R. § 1.116 has been received.

Proposed claims 49-60 presented within the Second Amendment After Final Rejection Under 37 C.F.R. § 1.116 and proposed claims 61-66 presented within the Third Amendment After Final Rejection Under 37 C.F.R. § 1.116 are not the subject of this appeal.

Assuming entry of at least the Second Amendment After Final Rejection Under 37 C.F.R. § 1.116, appellant hereby appeals the final rejection of claims 6, 25-29, 31, 37, and 43-48 which are presented in the Appendix.

IV. STATUS OF AMENDMENTS

Subsequent to the final rejection of November 4, 2003, an Amendment After Final Action (37 CFR Section 1.116) has been filed on February 4, 2004, a Second Amendment After Final Rejection Under 37 C.F.R. § 1.116 has been filed on March 8, 2004, and a Third Amendment After Final Rejection Under 37 C.F.R. § 1.116 has been filed on March 8, 2004.

The Advisory Action of February 25, 2004 indicated that the Amendment After Final Rejection Under 37 C.F.R. § 1.116 of February 4, 2004 had not been entered. No Advisory Action regarding the Second and Third Amendments After Final Rejection Under 37 C.F.R. § 1.116 has been received at the time of the filing of this Appeal Brief.

V. SUMMARY OF INVENTION

The present invention relates to a liquid crystal display (LCD) and, more particularly, to a matrix type liquid crystal display in which a driver circuit to apply a signal potential to each pixel is provided as an external circuit of a liquid crystal display panel.

At least figures 3 and 6 depict a display portion 10 (figure 6) in which a plurality of pixels 20 are two-dimensionally arranged at intersecting points of gate lines 11 as many as a plurality of rows and signal lines 12 as many as a plurality of columns which are wired in a matrix shape (figure 3). A plurality of driver circuits 14 for apply a signal potential to each pixel 20 in the display portion 10 through the signal lines 12 of the plurality of columns.

At least figures 7 and 8 depict time-divisional switches 46 for time-divisionally sending a signal potential that is outputted from each of the plurality of driver circuits 44 to the signal lines 42 of the plurality of columns, wherein a time-dividing number of the time-divisional switches is equal to 3.

As further described within the specification as originally filed, the number of output terminals of each of the plurality of driver circuits is set to a measure of the total number of signal lines of the plurality of columns (page 16, lines 14-18). The number of output terminals of each of the plurality of driver circuits 14 is set to a same number (figure 6). When a size of a frame portion adjacent to the display portion 10 is specified, the number (n) of output terminals of each of the plurality of driver circuits 14 is determined on the basis of the specified frame size by the number of lines which can be wired into a wiring region of the frame portion. When the total number of signal lines 12 of the plurality of columns that is decided by a display system is set to N, the number of driver circuits 14 is set to N/n, wherein the total number of signal lines 12 is different than the number (n) of output terminals (page 15, line 14 to page 16, line 24).

The plurality of driver circuits 14 are driver ICs arranged in an outside of a transparent insulating substrate on which the display portion 10 is formed.

At least figures 2, 3 and 5 depict a display portion 10 having a plurality of gate lines 11, a plurality of signal lines 12 and a plurality of pixels 20. A pixel 20 is located at an intersection of a gate line 11 and a signal line 12 (figure 3). A plurality of driver circuits 14 include at least one general driver circuit 14-1 to 14-25 and one remainder driver circuit 14-26. Each general driver circuit 14-1 to 14-25 has a plurality of general driver circuit output terminals, wherein a general driver circuit output terminal provides a signal potential to one of the plurality of signal lines 12 (figure 2). The remainder driver circuit 14-26 has a plurality of remainder driver circuit output terminals, wherein a remainder driver circuit output terminal provides another signal potential to another of the plurality of signal lines 12 (figure 5).

The quantity of the remainder driver circuit output terminals is defined as (S – (OP * (DC-1))), "S" being the quantity of the plurality of signal lines 12, "OP" being the quantity of the general driver circuit output terminals, and "DC" being the quantity of the plurality of driver circuits, wherein the quantity of the general driver circuit output terminals is different than the quantity of the remainder driver circuit output terminals (page 13, lines 10-26).

VI. ISSUES

The issues presented for consideration in this appeal are as follows:

Whether the Examiner erred in rejecting claims 3, 5-7, 11, 13-20, 23-29, 31, 37, 43-48 were rejected under 35 U.S.C. 102 as allegedly being anticipated by U.S. Patent 4,825,203 issued to Takeda et al. (Takeda).

This issue will be discussed hereinbelow.

VII. GROUPING OF CLAIMS

For purposes of this appeal brief only, and without conceding the teachings of any prior art reference, the claims have been grouped as indicated below.

Claim Groups:

Claims 3, 5, 7, 11, 13-20 and 23-24 stand or fall together.

Claim 6 stands or falls separately.

Claim 25-29, 37, 43-47 stand or fall together.

Claim 31 stands or falls separately.

Claim 48 stands or falls separately.

In Section VIII below, Applicant has included arguments supporting the separate patentability of each claim group as required by M.P.E.P. § 1206.

VIII. ARGUMENTS

In the Office Action of November 4, 2003:

The Examiner rejected claims 3, 5-7, 11, 13-20, 23-29, 31, 37, 43-48 under 35 U.S.C. 102 as allegedly being anticipated by Takeda.

For at least the following reasons, Appellant submits that this rejection is both technically and legally unsound and should therefore be reversed.

General Matters

M.P.E.P. 707.07(f) states that "the importance of answering such arguments is illustrated by *In re Herrmann*, 261 F.2d 598, 120 USPQ 182 (CCPA 1958) where the applicant urged that the subject matter claimed produced new and useful results. The court noted that since applicant's statement of advantages was not questioned by the examiner or the Board of Appeals, it was constrained to accept the statement at face value and therefore found certain claims to be allowable. See also *In re Soni*, 54 F.3d 746, 751, 34 USPQ2d 1684, 1688 (Fed Cir. 1995) (Office failed to rebut applicant's argument)."

The Examiner erred in rejecting claims 3, 5-7, 11, 13-20, 23-29, 31, 37, 43-48 under 35 U.S.C. 102 as allegedly being anticipated by Takeda.

This rejection is respectfully traversed for at least the following reasons.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Claim 6

Rejected claim 6, which has been amended to place that claim into independent form, is characterized in that the plurality of driver circuits are driver ICs arranged in an outside of a transparent insulating substrate on which the display portion is formed. However, a review of Takeda reveals that a "substrate" is not found therein. In addition, Takeda is silent as to the substrate being a "transparent insulating substrate".

Because a "substrate" or a "transparent insulating substrate" are not found within Takeda, all features within claim 6 are not found within Takeda. Thus, the final rejection of at least claim 6 is improper and premature as a result.

In addition, rejected claim 6 provide that when a size of a frame portion adjacent to the display portion is specified, the number (n) of output terminals of each of the plurality of driver circuits is determined on the basis of the specified frame size by the number of lines which can be wired into a wiring region of the frame portion, and when the total number of signal lines of the plurality of columns that is decided by a display system is set to N, the number of the driver circuits is set to N/n, the total number of signal lines being different than the number (n) of output terminals.

The Final Office Action cites elements q_1-q_N of Takeda as the plurality of driver circuits. While figure 1(A) of Takeda arguably depicts elements q_1-q_N at the output of shift register 31, the description found within Takeda fails to provide, with particularity, a written definition for elements q_1-q_N.

Instead, Takeda arguably teaches that "the column electrode drive circuit mainly comprises a shift register (31) which outputs a signal corresponding to the display pattern to each column electrode line" (figures 1(A),(B), column 4, lines 29-31), that "the signals required for sequential display are input to the gate circuit (37) from the shift register" (column 4, lines 59-61), and that "a shift register (31) that outputs signals to each column electrode line corresponding to the display pattern" (figure 5(A), column 6, lines 12-14). As shown above, Takeda arguably teaches

elements q_1-q_N as "signals" while failing to disclose, teach or suggest elements q_1-q_N as "a plurality of driver circuits".

Moreover, calculations provided within the Final Office Action arguably teach the total number of signal lines in Takeda as being ***the same as*** the number (n) of output terminals of each of the plurality of driver circuits. However, the claimed invention provides that the total number of signal lines ***is different*** than the number (n) of output terminals of each of the plurality of driver circuits.

Claims 3, 5, 7, 11, 13-20 and 23-24

While not conceding the propriety of these rejections, and in order to further the prosecution of the application, claims 3, 5, 7, 11, 13-20 and 23-24 have been canceled without prejudice or disclaimer of their underlying subject matter, rendering the rejection moot as to these claims.

Claims 25-29, 37, 43-47

Claim 25 and the claims dependent thereon comprise a plurality of driver circuits including at least one general driver circuit wherein a general driver circuit output terminal provides a signal potential to one of the plurality of signal lines. The plurality of driver circuits further includes one remainder driver circuit wherein a remainder driver circuit output terminal provides another signal potential to another of the plurality of signal lines.

The Final Office Action contends that Takeda depicts row electrodes 11-a as a plurality of gate lines 11-a and column electrodes 11-b as a plurality of signal lines 11-b. Thus, the Final Office Action identifies the row electrodes 11-a as the plurality of gate lines 11-a, and not as the plurality of signal lines.

But while figure 1(A) of Takeda arguably depicts plurality of driver circuits having a column electrode drive circuit 13 (column 4, line 23) providing signals to column electrodes 11-b (column 3, lines 4-6), and figure 3(A) of Takeda arguably depicts a row electrode drive circuit 121,122 (column 4, lines 11-12) providing signals to row electrodes 11-a (column 3, lines 1-2), Takeda fails to disclose, teach or suggest both the column electrode drive circuit 13 and the row electrode drive circuit 121,122 providing signal potentials to column electrodes 11-b.

Thus, Takeda fails to disclose, teach or suggest column electrode drive circuit 13 and the row electrode drive circuit 121,122 as the plurality of driver circuits found within claim 25 and the claims dependent thereon since the claimed plurality of driver circuits provide a signal potential to the plurality of signal lines whereas the row electrode drive circuit 121,122 of Takeda provides signal potentials to the row electrodes 11-a and not to the column electrodes 11-b.

The Final Office Action cites elements q_1-q_N of Takeda as the plurality of driver circuits. While figure 1(A) of Takeda arguably depicts elements q_1-q_N at the output of shift register 31, the description found within Takeda fails to provide, with particularity, a written definition for elements q_1-q_N. Instead, Takeda arguably teaches that "the column electrode drive circuit mainly comprises a shift register (31) which outputs a signal corresponding to the display pattern to each column electrode line" (figures 1(A),(B), column 4, lines 29-31), that "the signals required for sequential display are input to the gate circuit (37) from the shift register" (column 4, lines 59-61), and that "a shift register (31) that outputs signals to each column electrode line corresponding to the display pattern" (figure 5(A), column 6, lines 12-14). As shown above, Takeda arguably teaches elements q_1-q_N as "signals" while failing to disclose, teach or suggest elements q_1-q_N as "a plurality of driver circuits".

Also note that figure 1(A) of Takeda depicts buffer 36 as having only a single output Q_N, and not two (2) outputs as contended within the Office Action, and that a single signal q_N shown within figure 1(A) of Takeda corresponds only to a single output Q_N.

Moreover, claim 25 and the claims dependent thereon provide that the quantity of general driver circuit output terminals are different than the quantity of remainder driver circuit output terminals. But as shown within figure 1(A) there is the same quantity of outputs from each of the buffers 36, there is the same quantity of outputs from each of the analog switches 32, 34, and there is the same quantity of outputs from each of the gate circuits 37.

The Final Office Action further contends that each general driver circuit has a plurality of general driver circuit output terminals 36. But since each of the signals q_1-q_N of Takeda are uniquely associated with a buffer 36, this contention is inconsistent at least with the other contention regarding claim 25 made within the Final Office Action that elements q_1-q_N of Takeda are the plurality of driver circuits.

The Final Office Action asserts without provided any evidentiary support that there are two (2) remainder driver circuit output terminals, five (5) plurality of signal lines, three (3) general driver circuit output terminals, and two (2) plurality of driver circuits.

In response, this unsupported assertion amounts to nothing more than conclusions that are personal in nature because the cited prior art does not contain a sufficient teaching of how to obtain the desired result, or that the claimed result would be obtained if certain directions were pursued. In this regard, the teachings, suggestions or incentives supporting the rejection must be clear and particular.

As a rule, "assertions of technical facts in areas of esoteric technology must always be supported by citation to some reference work recognized as standard in the pertinent art and the appellant given, in the Patent Office, the opportunity to challenge the correctness of the assertion or the notoriety or repute of the cited reference." (Citations omitted). *In re Pardo and Landau*, 214 USPQ 673, 677 (CCPA 1982). The support must have existed at the time the claimed invention was made. *In re Merck & Co., Inc.*, 231 USPQ 375, 379 (Fed. Cir. 1986). Broad conclusory statements standing alone are not evidence.

Claim 31

The rejection of this claim is traverse at least for the reasons provided hereinabove with respect to claim 25 and for the following reasons.

Claim 31 includes a surplus connecting region that does not contribute to said display portion does not occur on the said display. However, Takeda fails to disclose, teach or suggest a surplus connecting region that does not contribute to the display portion which does not occur on the display. The Final Office Action cites elements 12, 13 and 15 of Takeda for this teaching. But in this regard, element 12 of Takeda contributes to the display portion as the row electrode drive circuit (Takeda at column 3, line 1), element 13 of Takeda contributes to the display portion as the column electrode drive circuit (Takeda at column 3, line 4), and element 15 of Takeda contributes to the display portion as the control circuit (Takeda at column 3, line 8).

Claim 48

The rejection of this claim is traverse at least for the reasons provided hereinabove with respect to claim 25 and for the following reasons.

Within claim 48, the plurality of driver circuits are driver integrated circuits arranged in an outside of a transparent insulating substrate on which said display portion is formed However, a review of Takeda reveals that a "substrate" is not found therein. In addition, Takeda is silent as to the substrate being a "transparent insulating substrate".

Conclusion

The Office Action fails to disclose, teach or suggest at least the above-noted features of the claimed invention at the time the invention was made, and therefore, does not anticipate Applicant's invention or render it obvious.

Thus, the claims are considered allowable for the same reasons discussed above, as well as for the additional features they recite.

Reversal of the Examiner's decision is respectfully requested.

IX. CLAIMS INVOLVED IN THE APPEAL

A copy of the claims involved in the present appeal is attached hereto as Appendix A.

If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

Dated: April 2, 2004

Respectfully submitted,

By_____

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APPENDIX A

6. A liquid crystal display comprising:

a display portion in which a plurality of pixels are two-dimensionally arranged at intersecting points of gate lines as many as a plurality of rows and signal lines as many as a plurality of columns which are wired in a matrix shape;

a plurality of driver circuits for applying a signal potential to each pixel in said display portion through the signal lines of said plurality of columns; and

time-divisional switches for time-divisionally sending a signal potential that is outputted from each of said plurality of driver circuits to the signal lines of said plurality of columns,

characterized in that a time-dividing number of said time-divisional switches is equal to 3,

the number of output terminals of each of said plurality of driver circuits is set to a measure of the total number of signal lines of said plurality of columns,

the number of output terminals of each of said plurality of driver circuits is set to a same number,

when a size of a frame portion adjacent to said display portion is specified, the number (n) of output terminals of each of said plurality of driver circuits is determined on the basis of said specified frame size by the number of lines which can be wired into a wiring region of said frame portion,

when the total number of signal lines of said plurality of columns that is decided by a display system is set to N, the number of said driver circuits is set to N/n, said total number of signal lines being different than said number (n) of output terminals,

characterized in that said plurality of driver circuits are driver ICs arranged in an outside of a transparent insulating substrate on which said display portion is formed.

25. A liquid crystal display comprising:

a display portion, said display portion having a plurality of gate lines, a plurality of signal lines and

a plurality of pixels,

a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines; and

a plurality of driver circuits, said plurality of driver circuits including at least one general driver circuit and one remainder driver circuit,

each said at least one general driver circuit having a plurality of general driver circuit output terminals, a general driver circuit output terminal of said plurality of general driver circuit output terminals providing a signal potential to one of said plurality of signal lines,

said remainder driver circuit having a plurality of remainder driver circuit output terminals, a remainder driver circuit output terminal of said plurality of remainder driver circuit output terminals providing another signal potential to another of said plurality of signal lines,

the quantity of said remainder driver circuit output terminals being defined as (S – (OP * (DC-1))), "S" being the quantity of said plurality of signal lines, "OP" being the quantity of said general driver circuit output terminals, and "DC" being the quantity of said plurality of driver circuits, and

said quantity of said general driver circuit output terminals being different than said quantity of said remainder driver circuit output terminals.

26. A display according to claim 25, wherein each driver circuit of said plurality of driver circuits is separate and distinct from another driver circuit of said plurality of driver circuits.

27. A display according to claim 25, wherein said plurality of pixels is arranged in a two-dimensional matrix shape.

28. A display according to claim 25, wherein said pixel of said plurality of pixels includes a transistor, a gate electrode of said transistor being electrically connected to said gate line, a source/drain of said transistor being electrically connected to said signal line.

29. A display according to claim 25, wherein said plurality of gate lines is a plurality of rows and said plurality of signal lines is a plurality of columns.

31. A display according to claim 25, wherein a surplus connecting region that does not contribute to said display portion does not occur on the said display.

37. A display according to claim 25, wherein an output terminal of said plurality of driver circuits is electrically connected to an input terminal of a time-divisional switch, said time-divisional switch providing a de-multiplexed signal potential to said signal line, said de-multiplexed signal potential being a signal potential for one of a plurality of primary colors that is time-divided from another signal potential for another of said plurality of primary colors and supplied to said signal line.

43. A display according to claim 37, wherein said plurality of primary colors is a first primary color, a second primary color and a third primary color.

44. A display according to claim 25, wherein said quantity of general driver circuit output terminals is greater than said quantity of remainder driver circuit output terminals.

45. A display according to claim 25, wherein the sum total of general driver circuit output terminals and said remainder driver circuit output terminals is equal to said plurality of signal lines.

46. A display according to claim 25, wherein said plurality of driver circuits include more than one said general driver circuit.

47. A display according to claim 46, wherein each said general driver circuit has an equal number of general driver circuit output terminals.

48. A display according to claim 25, wherein said plurality of driver circuits are driver integrated circuits arranged in an outside of a transparent insulating substrate on which said display portion is formed.